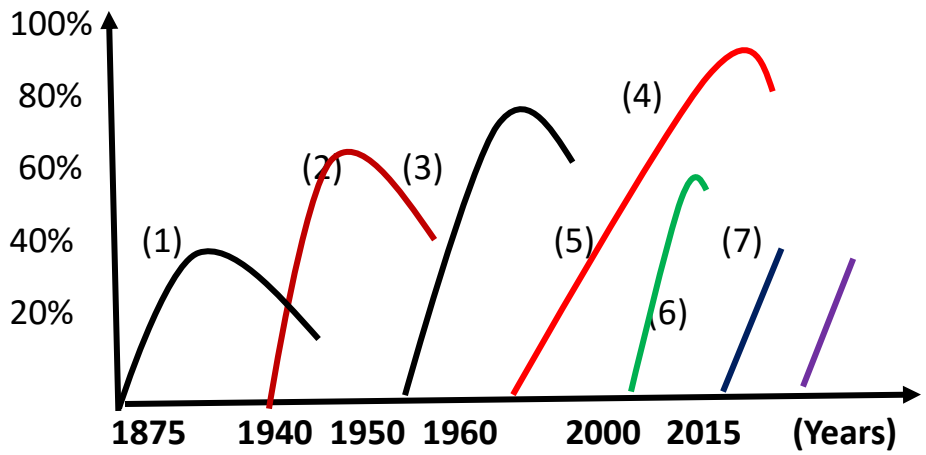
Examination Questions

Question (1)

Draw and explain how the, electronics technology developed as a function with the reliability of components manufactured to realize the aspirations of modern man that even today.

Curves in figure (I - 3) shows, electronics technology as a function with the reliability of components manufactured to realize the aspirations of modern man that even today.



1- Silicon Photo cells (Semiconductor Materials)

2- Vacuum Tube Technology

3- Semiconductor Technology

4- Integrated circuits (Small – Medium – Large – Super large)

5- Optical Electronic (LASER) Technology

6- Superconductor Technology

7- Nano technology

In the fifty years since the emergence of vacuum tube technology human achieved many technological systems and control what considered dreams to

previous generations. The development and introduction of advanced technologies for electronics science and engineering are natural extension of semiconductor technology, including different types of transistors that appeared in 1951 and integrated circuit technology for small and medium-sized and very large and super large in1960 and still evolving stand-up.

Now it is performing basic microprocessor pattern on a small slice of silicon, and skip the stages where recently announced that it has access to the high density of elements with more than 500 thousand devices per one cm^2. and thus, might develop services in multiple areas and did not stand when it also announced a few years back to vacuum tube technology where through this technology can reach some difficult applications implemented with semiconductor technology and integrated circuits where it is possible to implement 100 valve in one cm^3. No wonder we are in the third electronics technology generation, recently announced the emergence of technologies as, optoelectronics, and superconductive materials technology. In 50 years only began the true history of electronics. Not forget the Nano-electronics. the future promise for achieving dreams. we are unable to implement modern technology thus it requires the concept of contemporary technology and control them, so that we can receive future technology without fear and God only knows.

Question (2)

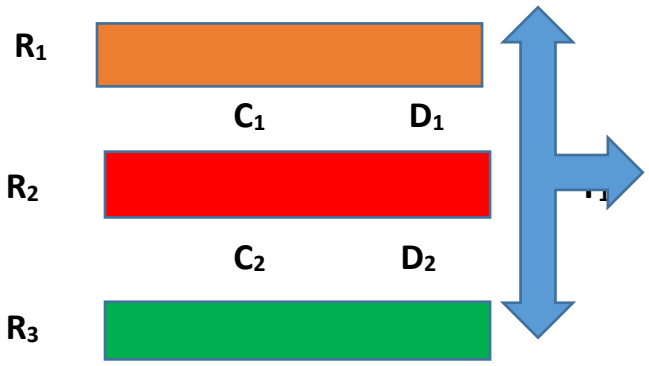
Can you Explain with drawing a very simple model to the meaning of integrated circuit?

Solution

Could be simpler to say that slice of silicon, has resistance to measure. As example, R1 (is one of the electronic elements). If we used two slices placed one over the other to form two layers – so we have two resistances R1 and R2 – between the two layers, can be free air however were attached (filled with air or any electrical insulation material) so it can be represented with a capacitance C1 and another element called a binary or diode (D1).

This means that we have through the semiconductor segments one over the other to get number of four electronic elements R1, R2, C1, and D1. Apply third slice on

previous. it means R1, R2, R3, C1, C2, D1, D2 and also get a new component a transistor T1, became number of three resistances, two capacitors, two diodes, and one transistor which means eight electronic elements. Each element depends on the rest of the Group and this is the basis of the concept of integrated elements. In addition, even understand the idea – imagine the configuration as shown in figure (I -4).



Question (3)

We know that, for electronic uses, the most important property of semiconductor material is that its conductivity be modulate by external signals, can you determine such parameter that effect the conductivity?

Solution

1-Conductivity (σ) directly proportional to the number of free charge carriers, negative electrons or positive holes, so σ regulates current in the device.

2-Concentration of electrons (n) or holes (p) is directly proportional to the electric field (ε) applied.

3-Light, heat, mechanical stress, magnetic fields, affect concentration of electrons (n) or holes (p).

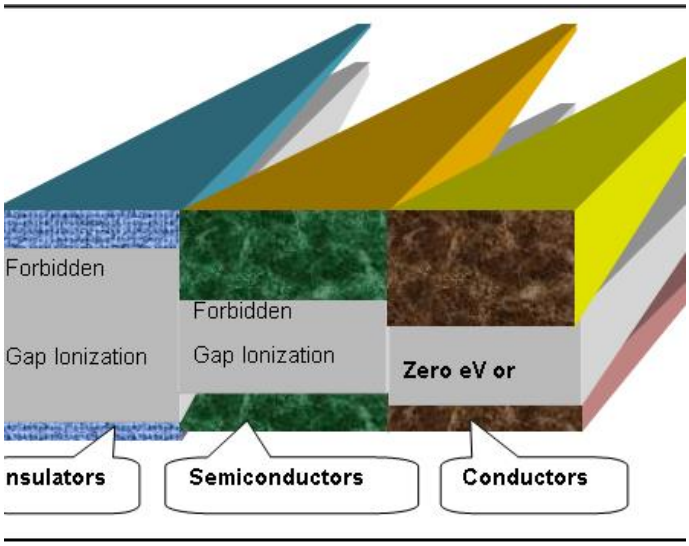
4- Adding small quantities of dopants varies carrier concentration and the conductivity.

Question (4)

The energy levels of electrons grouped into bands separated by forbidden gap , compare between such energy bands in solid by explanation and drawings?

Solution

The lowest Energy State named valance band, and the highest one is the conduction band. In term of energy consideration this means that, conduction is possible only if we can impart kinetic energy to an electron or hole among the solid. If electric field ε applied, these electrons move toward the positive side, and electric current flow. The material classified for three main types, Conductors, Insulator, and Semiconductors. The corresponding energy bands for these classifications are shown in figure.



In Conductors, the valance electrons are free to move and constitute a sea of electrons, which are free to move upon the application of even small electric field. The two bands for aluminum as an example for conductor are overlapped, thus there is no energy gap, so it is possible to move the top most electron to the next levels, i.e., it is possible to impart a kinetic energy to the electron. Hence, conduction is possible. In insulator, such as a SiO_2, the valance electron form strong bonds between neighboring atoms;

Question (5)

Each electron in the energy levels of semiconductors has equal probability to occupy any energy state, due to Pauli exclusion, can you explain this exclusion?

Solution

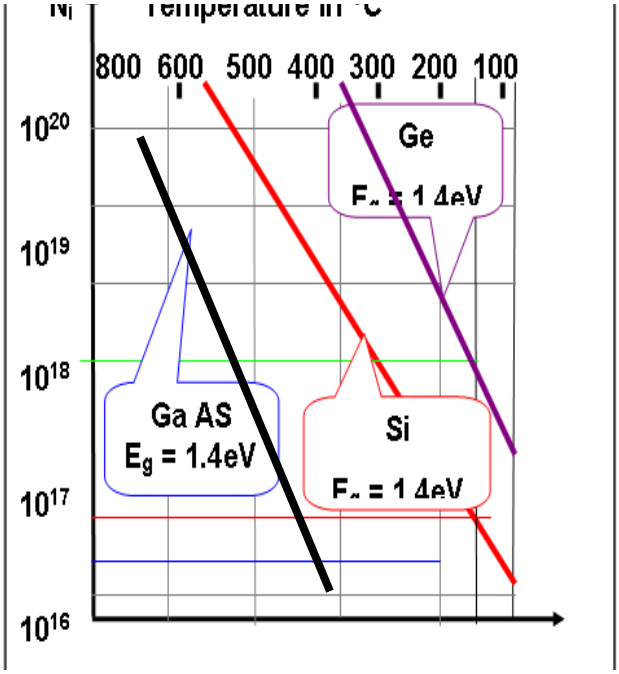
Due to Pauli exclusion, since in absolute temperature, all charge carriers are frozen and founded in the lowest energy levels, if temperature increased the electrons activate and represents in higher levels, each electron has equal probability to occupy any energy state where no two electrons have the same Energy State in the same atom in the same time.

Question (6)

Show that, intrinsic concentration density N_i for different semiconductor materials, is in a function of temperature

Solution

The figure, shows three different semiconductor materials, Ge- Si- and Ga As,



from figure, we can indicate:

1- Intrinsic concentration densities increase very sharply with temperature.

2- Intrinsic concentration density decreases very sharply with energy gap.

$$E_a = {}^{1}\!/_{2} \; E_g \qquad Eq.1.3$$

This summarized by the exponential temperature dependence

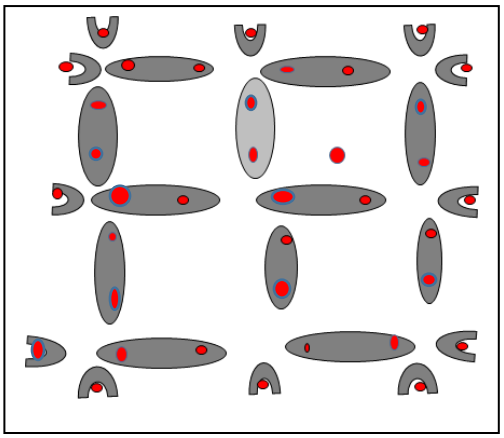
$$n_i \propto e^{\left(-E_a/KT\right)} \qquad Eq.1.2$$

Question (7)

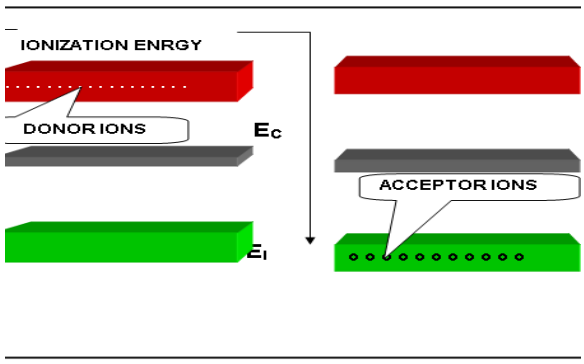
Explain how we can get N – Type Material, Draw Structure Model and Energy Band Representation of such material?

Solution

If we add, a dopant has five valance electrons to which has four, like Phosphorus, Antimony, Arsenic, the extra electron of the dopant cannot fit in the regular bond arrangement of the Ge or Si lattice.



The ionization energy of such dopant is about 0.05 eV. At room temperature, there is enough energy to supply this amount. Column V materials in Ge or Si will be ionized at room temperature.



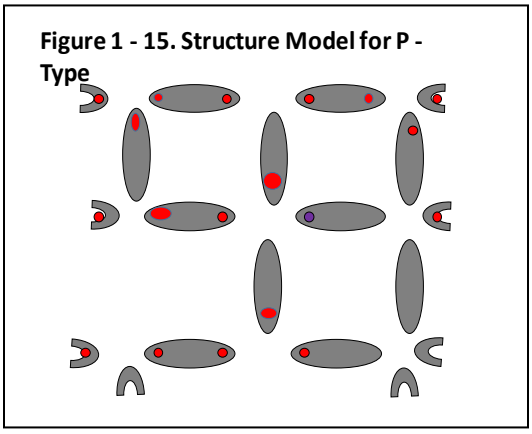
Question (8)

Explain how we can get p – Type Material, Draw Structure Model and Energy Band Representation of such material?

Solution

Semiconductor materials such Ge or Si doped with three valance electron materials, column III such as Born, Aluminum, Gallium, Indium, Sense column III materials has one less electron than Ge or Si, we can consider it to carry a hole.

This hole removed easily with ionization energy of 0.05 eV.



Question (9)

What is meant by the expression complete ionization?

Solution

In case of complete ionization, the density of holes equals to density of the acceptor ions denoted by negative charge slightly above the acceptor, band energy level.

Question (10)

How you can differnate between the both conduction material types?

Solution

In the n-type material, the concentration of electrons is much larger than of holes (n>p), and the current is due to electrons and the conduction is occurred in the conduction band. In the p-type material, the concentration of holes is much larger than of electrons (p>n), and the current is due to holes, and the conduction is occurred in the valance band.

Question (11)

How you can compare between intransic , extrinsic, compensated material?

Solution

- **In the case of Intransic material, electron concentration is equal to hole concentration (n = p), and Fermi level is in the middle of energy gap**
- **In the case of Extrinsic material, electron concentration is not equal to hole concentration. In the case of n-type (n > p), where the conduction occurred by electrons in conduction band and Fermi level is shifted upward in the direction of conduction band, and a new level named donor level, E_D, exists. If (p>n), results p-type material, conduction occurred by holes in valance band and a new level acceptor level, E_A, exists.**
- **In the case of compensated material, $N_A^- = N_D^+$ we have extrinsic material have the same properties of intrinsic**

Question (12)

How you can compare between majority, and minority charge carriers in the Extrinsic material?

Solution

In the electrical neutrality law n_i^2 =np ,

- **In the n-type , electrons is majority and it can be written as n_n and p the holes is minority and it can be written as p_n, so we can write the electrical neutrality law as : $n_i^2=n_n\, p_n$,**

$$p_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D}$$

For p-type, p is majority and it written as p_p, and electrons are minority and it written as n_p, so we can write electrical neutrality law for p-type as:

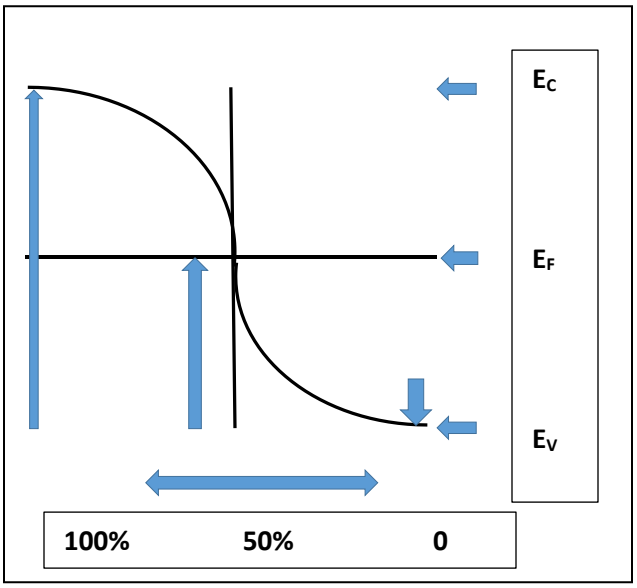
$$n_i^2 = p_p\, n_p \ , \ n_p = \frac{n_i^2}{P_p} = \frac{n_i^2}{N_A}$$

Question (13)

what determine the probability that a given energy state occupies by electron?

Solution

The accurate number of electrons dN having a value of energy in each range of energy state E+ ∆E at absolute temperature can be expressed by FERMI as:



$$dN = \frac{C\sqrt{E}\, dE}{e^{(E-E_F)/KT}+1}$$

E_f is defined as the highest electronic energy at absolute temperature. At E = E_f, the probability of electron occupancy is 50%. It is important to note that, at 0K all the charge carriers frozen and lies in the lowest level of the energy gap. In conduction band, there is large number of states has small probability of occupation, there will be only a few electrons in the conduction band. In contrast, there many states in valance band, most of them occupied and the probability of occupation is unity, so there will be only a few unoccupied energy states in valance band.

Question (14)

When the FERMI level located in middle of the energy gap?

Solution

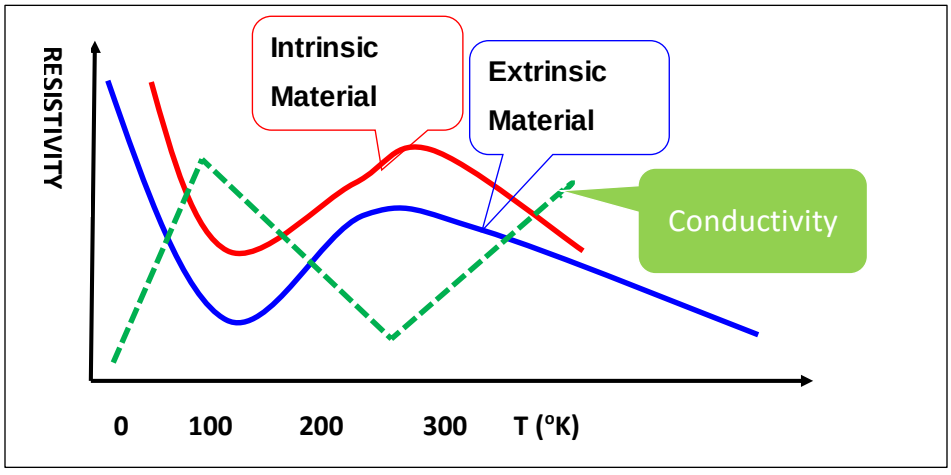
FERMI level located in middle of the energy gap, If the number of energy states in conduction and valance band are the same. In addition, if the number of electrons in conduction and valance band are the same.

Question (15)

How you can explain the dependence of conductors and semiconductors with the temperature increasing?

Solution

In metals, Conductivity decreases by increasing temperature due to greater frequency of collisions of electrons.



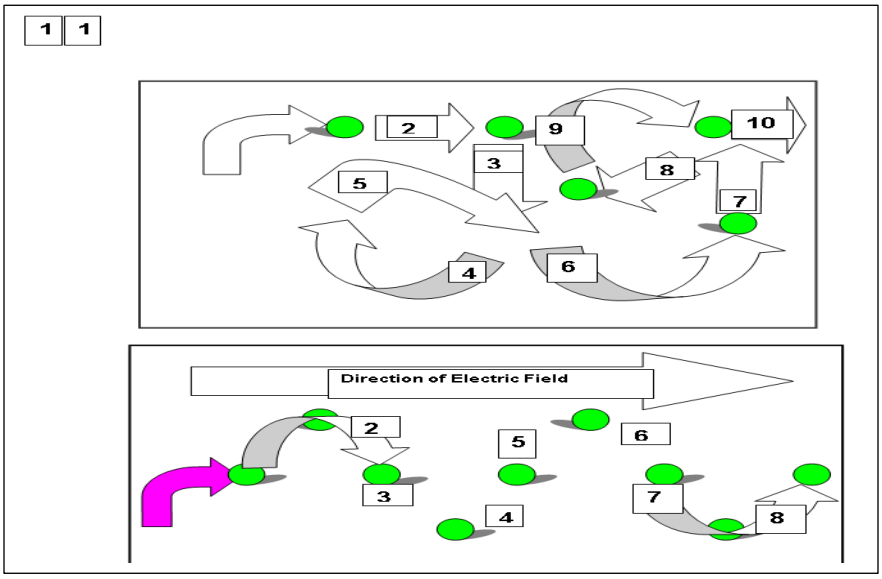
In semiconductor, as shown, at low temperature, the charge carriers are frozen and the resistivity is extremely high, as the temperature raises, increasing fraction of carriers to ionize and the resistivity decreases rapidly because of increasing the ionized charges. When temperature is sufficiently high, most of dopants are completely ionized. The Conductivity begins to decrease and the resistivity is increased again just as in metals. At still higher temperature, there is further sharp decrease in resistivity due to appreciable excitation of all carriers and crossing the energy gap.

Question (16)

How the electron behaves at absolute temperature in a perfect semiconductor sample without and with subjected external electric field

Solution

When an electron introduced without subjected external electric field at absolute temperature in a perfect semiconductor sample. The electron will move freely random through the crystal as shown in figure. At room temperature, valance electrons are liberated by random motion through the crystal. Under thermal equilibrium condition, the random motion of electrons leads to zero current in any direction. The thermal vibration introduced due to collisions called scattering. The scattering phenomena increased as temperature increases for a maximum scattering velocity.



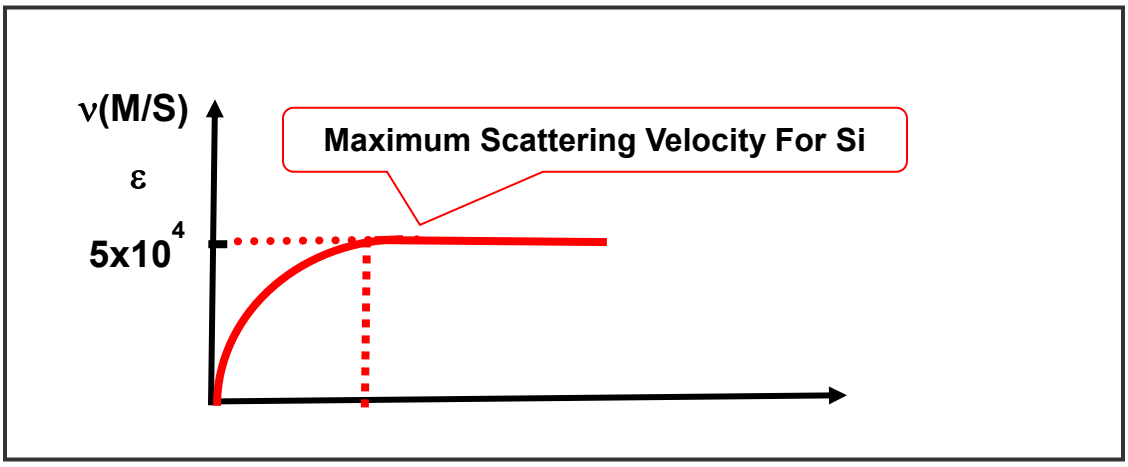
If we apply electric field to the crystal, the electrons gain a force qε toward the positive pole as shown, and moves with acceleration given by:

$$a = -\frac{q\,\varepsilon}{m}$$

And current flow. After time (τ), the electrons suffer of collisions decreases velocity (ϑ) between each two consecutive collisions as $\Delta\,\vartheta$ = a τ, produces what is called drift velocity (ϑ_d) .

$$\vartheta_d = \Delta\,\vartheta = \mu\,\varepsilon$$

By increasing the subjected field, the drift velocity increases, due to the increasing of kinetic energy of the electrons. When electric field is higher increased, a critical value developed and reaches maximum scattering velocity; this velocity is not more increased by increasing electric field,



Question (17)

What is the main factors affecting the mobility of charge carriers in semiconductors?

Solution

There are three main factors affecting the mobility of charge carriers in semiconductors, they are:

Temperature: As temperature increases, the thermal kinetic energy increases the vibration of atoms and the charge carriers suffer from Collisions, the dependence of mobility in temperature given by:

$$\mu_L = KT^{-3/2}$$

Impurities: The scattering of charge carriers results from the presence of ionized donors or acceptors or impurities. This charged centers will deflect the motion of carriers by the electrostatic forces between two bodies, so the density of such centers affect the velocity; it is also being noted that, the impurity scattering decreases as temperature increases.

$$\mu_I = \frac{KT^{3/2}}{N_I}$$

Dislocations:

Dislocation is atomic misfit, where atoms not probably arranged, so it has a considerable role of scattering carriers. For example, in germanium, the dislocations behave as acceptors, and the mobility affects by:

$$\mu_D = KT$$

Now if we combine these three parameters, we have a general expression to determine such effects in mobility of charge carriers.

$$\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I} + \frac{1}{\mu_D} = \alpha_L T^{3/2} + \alpha_I T^{-3/2} + \alpha_D T^{-1}$$

Question (18)

How is the drift and diffusion currents produced in semiconductor sample?

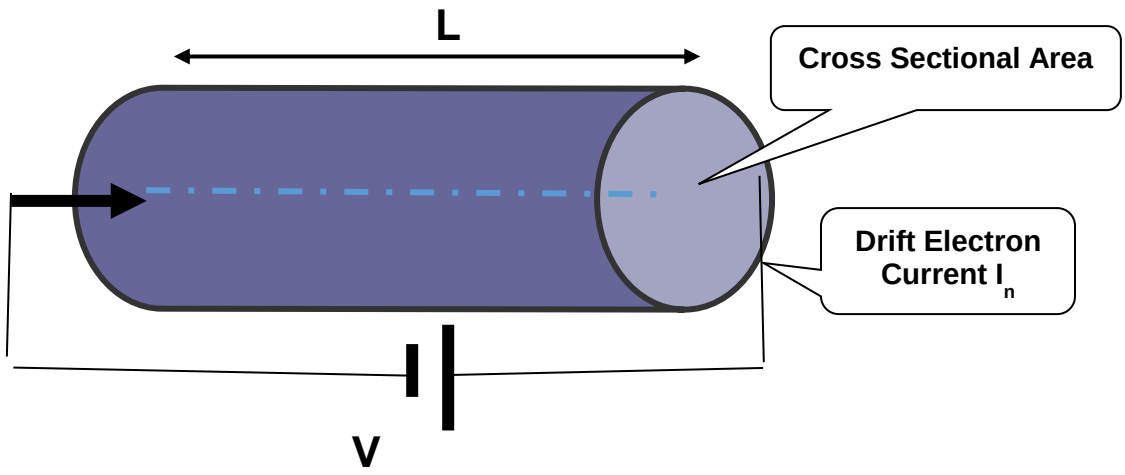
Solution

The drift current due to Transport of charge carriers under electric field produces a drift current. The current flow in a sample having electron concentration (n) given by:

$$I_n = -q\, n\, \vartheta_d\, A$$

Substitute in the drift velocity, gives:

$$I_n = -q\, n\, (\mu_n\, \varepsilon)\, A$$



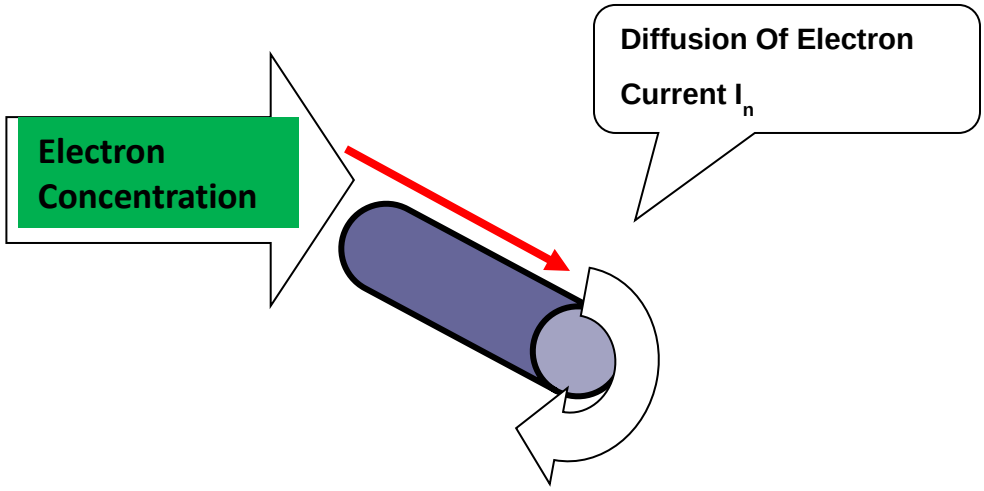
The same steps can be done to determine the drift current due to the hole component in p-type material,

$$I_p = q\, p\, (\mu_{np}\, \varepsilon)\, A$$

In semiconductor, both carriers are included, so:

$$I_T = q\, A\, \varepsilon\, (n\, \mu_n + p\, \mu_p)$$

THE DIFFUSION CURRENT due to diffusion of charges, the concentration of charge carrier is not uniform. Diffusion of electrons or holes results from their movement from higher concentration to lower concentration with gradient d/dx where concentration of carriers is not distributed uniform and varies with distance x.



So that, the diffusion current due to electrons given by:

$$I_n = q\,A\,D_n\,\frac{\partial\,N}{\partial\,x}$$

And, the diffusion current due to holes is given by:

$$I_p = -\,q\,A\,D_p\,\frac{\partial\,P}{\partial\,x}$$

The total current of electrons and holes components given by the summing of its diffusion and drift currents as:

$$I_n = qA\left(n\,\mu_n\,E + D_n\,{}^{\partial n}/_{\partial x}\right)$$

$$I_p = qA\left(p\,\mu_p\,E + D_p\,{}^{\partial n}/_{\partial x}\right)$$

Question (19)

What is the parameters considered To calculate the flux (F) at a position (x), in semiconductor sample?

Solution

To calculate the flux (F) at a position (x), in semiconductor sample, it is average of fluxes at positions (x – a/2) and at (x + a/2), these two fluxes given by ($f_1 - f_2$), and ($f_3 - f_4$).Consider component (F_1), is product of:

1. Intensity per unit area for impurities (charges) at the potential valley at (x – a).
2. The probability of a jump of any of these impurities (charges) to the next valley at position (x)
3. The frequency of attempted jump (ν)

Thus, we can write:

$$F_1 = [a\,C\,(x-a)]\,exp - \frac{q}{K\,T}\left(W - \frac{1}{2}\,a\,\epsilon\right)(\nu)\;Eq\;(1-90)$$

Where, $[a\,C\,(x-a)]$ is the density per unit area of the particles situated in the valley at (x – a). The exponential factor is the probability of a jump from

the valley at (x – a) to the valley at position (x), and (ν) is frequency of attempted jump note that, the lowering of the barrier due to the electric field (ε). Similar formulas can be written for (F_2), (F_3), and (F_4). By combined them to give a formula for the flux (F) at position (x),

$$F(x) = -\left(\nu\, a^2\, e^{-qW/KT}\right)\frac{\partial C}{\partial x}\, cosh\, \frac{q\, a\, \varepsilon}{2\, KT} + \left(2\, a\, \nu\, e^{-qW/Kt}\right) C\, sinh\, -\frac{q\, a\, \varepsilon}{2\, KT}$$

As extremely important, limiting from of this equation is obtained for the case when the electric field is relatively small, i.e., ε «KT/q a. In this case, we can expand the cosh and the sinh terms in the equation. Noting that cosh (x) = 1 and sinh (x) = x for x → 0, this results in the limiting form of the flux equation for a positively charged spices.

$$F\,(x) = \; -D\,\frac{\partial\, C}{\partial\, x} \; + \; \mu\, \varepsilon\, C \quad ,$$

Chapter two

Question (19)

How a pn junction is formed?

Solution

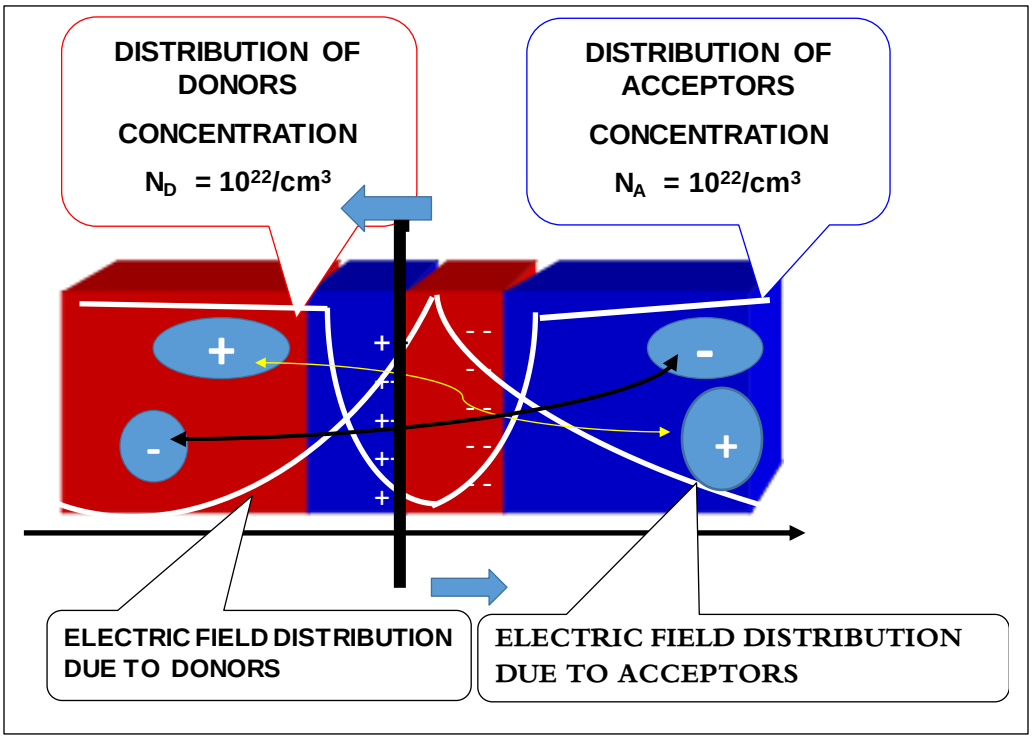
If two pieces of semiconductor materials with different conduction type are brought together in a contact, a junction is formed. Before contact there is a large electron concentration in the n-side and a large hole concentration in the p-side. After the two sides are brought into contact, electrons are diffused from the n-side to the p-side and holes are diffused from the p-side to the n-side. However, each electron that diffuses into the p-side leaves a positively charged donor atom behind in the n-side, likewise the holes that diffuse into the n-side leaves a negatively charged acceptor atom behind in the p-side. An electric field is built-up between the ionized donors and acceptor atoms in such a direction as to oppose further diffusion of electrons and holes and the system comes into equilibrium statement.

Question (21)

How pn junction comes in equilibrium statement?

Solution

If two pieces of semiconductor materials with different conduction type are brought together in a contact, a junction is formed. Before contact there is a large electron concentration in the n-side and a large hole concentration in the p-side. After the two sides are brought into contact, electrons are diffused from the n-side to the p-side and holes are diffused from the p-side to the n-side. However, each electron that diffuses into the p-side leaves a positively charged donor atom behind in the n-side, likewise the holes that diffuse into the n-side leaves a negatively charged acceptor atom behind in the p-side. An electric field is built-up between the ionized donors and acceptor atoms in such a direction as to oppose further diffusion of electrons and holes and the system comes into equilibrium statement.



Question (22)

Compare between symmetrical and unsymmetrical pn junctions?

Solution

- **Symmetrical junctions have equal and opposite doping on two sides, to the left of junction, Where $N_D = N_A$,$X_m = X_n + X_p$, and $X_n = X_p$**

Question (23)

Why the depletion region acts as insulating region

Solution

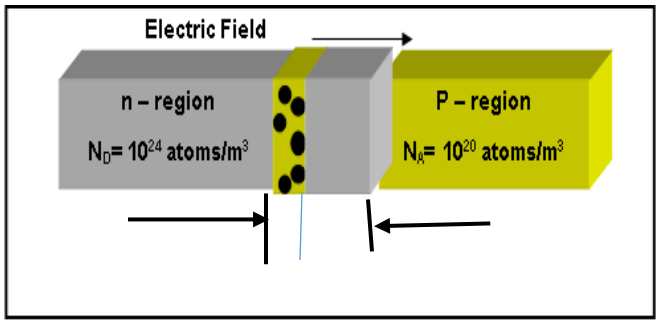
The depletion region acts as insulating region, since it contains no mobile carriers.

Question (24)

How you imagine the developing of the depletion region X_m for unsymmetrical pn junction?

Solution

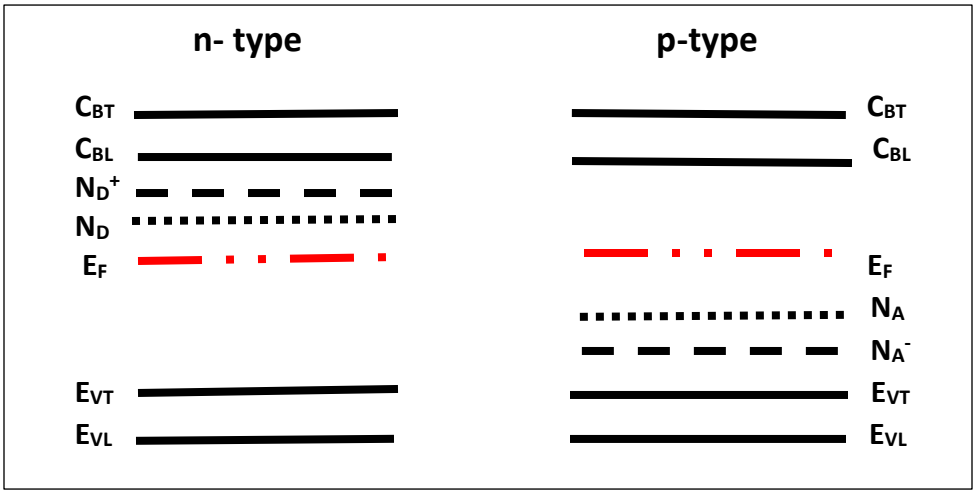
for unsymmetrical pn junction, for example n – material (n^+- p). Most of depletion layer extends into the side has the lowest concentrations. It realized, that charge neutrality must maintained as many positive charges as negative charges must presented in space charge of the depletion region.



Question (25)

Draw a block energy band diagram for np junction, showing all the energy levels and its location in the two sides?

Solution



Note, acceptor levels in the p-type side and the donor levels in the n-type side, most of them are ionized at room temperature (N_D^+ and N_D^+) . Since equilibrium is a condition that cannot support current flow in an external wire joining the p and n regions, the energy of electrons and holes must be equal in the two regions. The Fermi level must be a single level through the material.

Question (26)

Why the depletion layer in pn diode is considered as the heart of the diode?

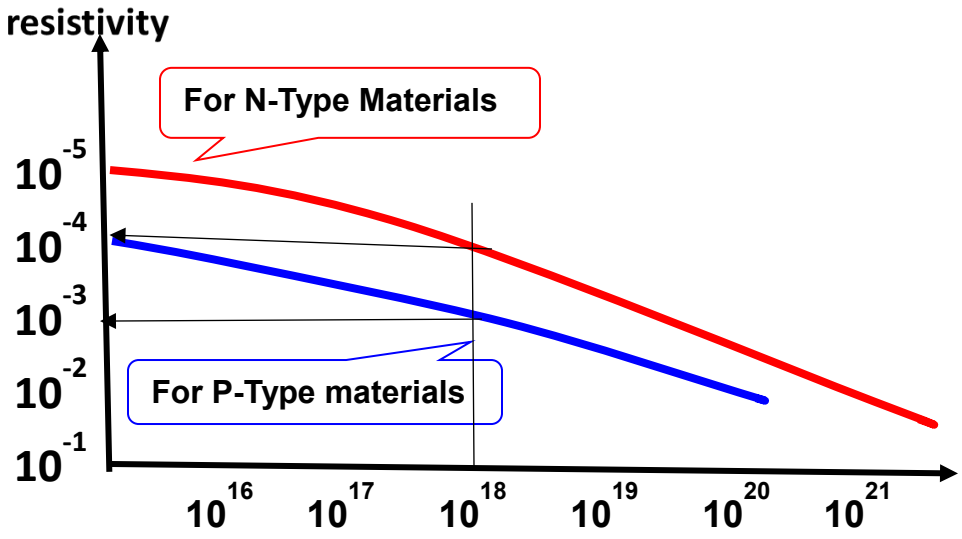
Solution

The depletion layer in pn diode is considered as the heart of the diode, since all the electrical phenomena are occurred.

Question (27)

At the same concentration of electrons in a sample, and the same concentration of holes in a sample, we find the electron current is greater than the hole current, It seems that the conduction is due to electrons, explain such phenomena?

Solution



$$I_T = q\,A\,\varepsilon\,(n\,\mu_n + p\,\mu_p)$$

In intrinsic, $n = p = n_i$, note that $\mu_n > \mu_p$, so in an intrinsic material the electrons contribute more to conductivity than holes. It seems that the conduction is due to electrons, so the conduction in intrinsic material considered as in n-type material. So, if we consider the cross-sectional area A for the sample are equal and ε in relation with the mobility , Let us consider the value of ($q\,A\,\varepsilon$) in the current equation which simplified to $I_T = (n\,\mu_n + p\,\mu_p)$ and the material under consideration has n = p , then $I_T \;\alpha\; (\mu_n + \mu_p)$, and since $\mu_n > \mu_p$, then we neglect the current due to holes and the total current is depend only with μ_n and the total current considered as electron current $I_T \;\alpha\; (\mu_n)$

Question (28)

In symmetrical pn junction , we find the electron current is greater than hole current, and we consider that the current due to electrons neglecting the hole current, explain such phenomena

Soluton

As in Question (27)

Question (29)

Why we consider that the current in intrinsic sample as as in n-type material?

Solution

$$I_T = q\,A\,\varepsilon\left(n\,\mu_n + p\,\mu_p\right)$$

In intrinsic, $n = p = n_i$, note that $\mu_n > \mu_p$, so in an intrinsic material the electrons contribute more to conductivity than holes. It seems that the conduction is due to electrons, so the conduction in intrinsic material considered as in n-type material. So, if we consider the cross-sectional area A for the sample are equal and ε in relation with the mobility , Let us consider the value of ($q\,A\,\varepsilon$) in the current equation which simplified to $I_T = \left(n\,\mu_n + p\,\mu_p\right)$ and the material under consideration has n = p , then $I_T \;\alpha\; \left(\mu_n + \mu_p\right)$, and since $\mu_n > \mu_p$, then we neglect the current due to holes and the total current is depend only with μ_n and the total current considered as electron current $I_T \;\alpha\; (\mu_n)$

Question (30)

In reverse bias condition, the current will disappear, explain?

Solution

In reverse bias condition, the current will disappear, since the holes in the p - side, and electrons in the n - side are move away from the junction. Because in the reverse bias the barrier voltage is increased and charge carriers is decreased and the depletion layer thickness increased. And constitute small current known as reverse saturation current I_R or I_o or I_s .

Question (31)

How you can explain the forward and reverse bias condition?

Solution

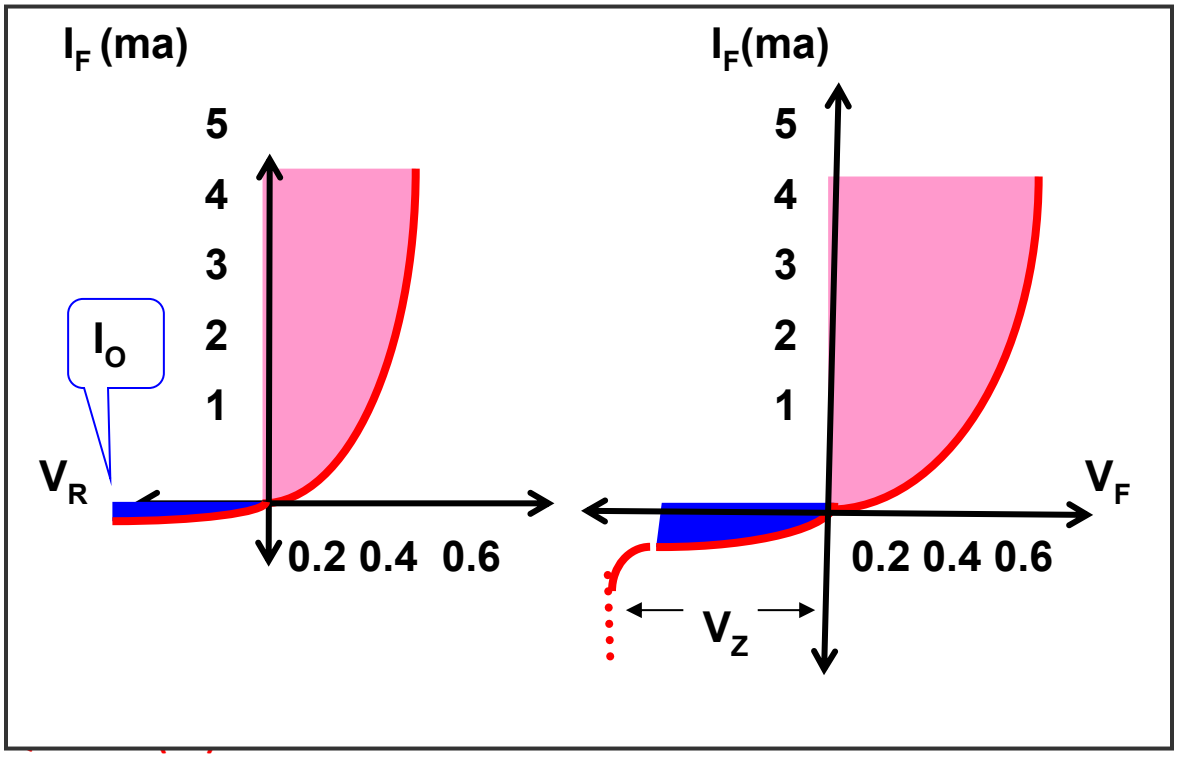
In forward bias, height of potential barrier decreased than the nominal value of V_T increases flow of majority carrier's (p_P), and (n_n), and the charge carriers increased and current flow depend with V_F

In reverse bias, height of potential barrier increased than the nominal value of V_T, reduces flow of majority carrier's (p_P), and (n_n), also reduce flow of minority carriers (p_n), and (n_p). and current will be equal reverse saturation current (I_R) , it is a constant not depend with V_R until certain limit. Until reverse voltage becomes very large, then at critical voltage a large current surge through the diode and junction breakdown is occurred. It can damage the diode

Question (32)

Draw the IV characteristics for the diode at both the forward and reverse bias condition?

Solution



Question (32)

Question (33)

What are the currents exists in the diode , can you write the equation for each component?

Solution

there are two components of current density flowing across the junction.

- **Current density component J_{1n} is the component of the current density that flows down the potential barrier with the electron flowing from p-region to n-region and it is the drift current density due to the free electrons under the influence of the field because the potential barrier and J_{1n} may be written as:**

$$J_{1n} = qn\mu_n\varepsilon \qquad (2.2)$$

Current density component J_{2n} flow of electrons from n-region where free electrons are majority carriers to p-region where they become minority current flows due to diffusion, thus,

$$J_{2n} = qD_n\frac{dn}{dx} (2.3)$$

When applied, voltage is zero, sum of the two components is equal to zero, hence:

$$J_{1n} + J_{2n} = qn\mu_n\varepsilon + qD_n\frac{dn}{dx} = 0 \quad (2.4)$$

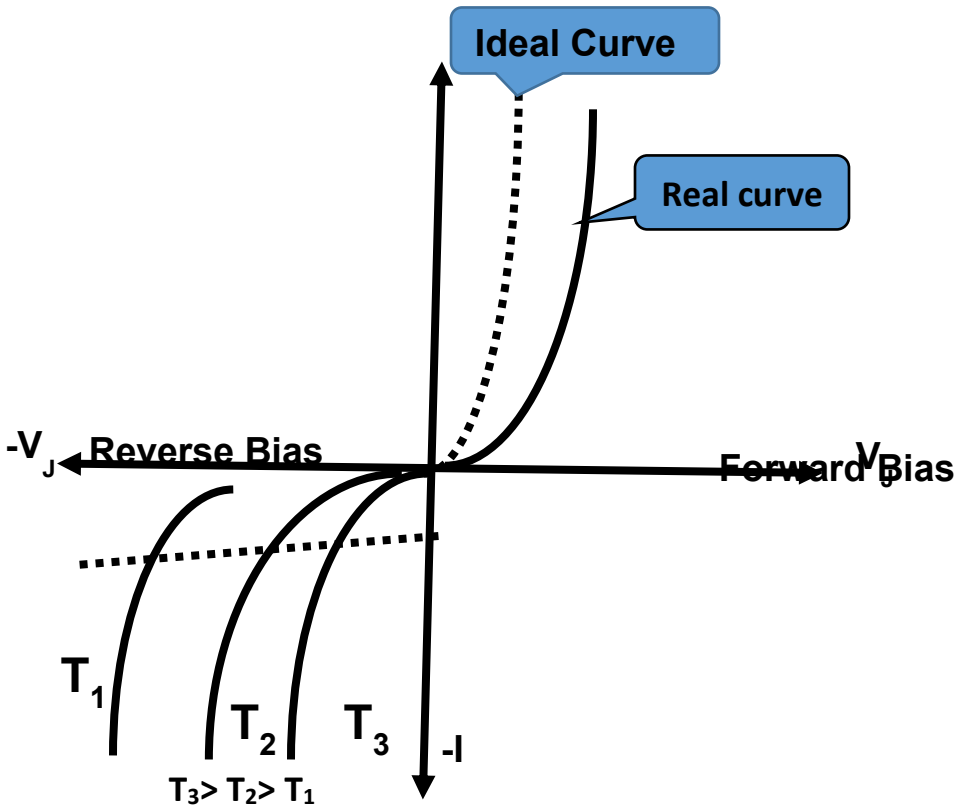
$$J_{1p} + J_{2p} = qp\mu_{np}\varepsilon + qD_p\frac{dp}{dx} = 0$$

So, there are four current components Two diffusion currents ($qD_n\frac{dn}{dx}$ and $qD_p\frac{dp}{dx}$) and two drift currents ($qn\mu_n\varepsilon$ and $qp\mu_{np}\varepsilon$). The total current flowing will be nearly equal to sum of electron and hole diffusion currents at junction.

Question (34)

Draw the IV characteristics for the diode at both the forward and reverse bias condition as dependent on temperature?

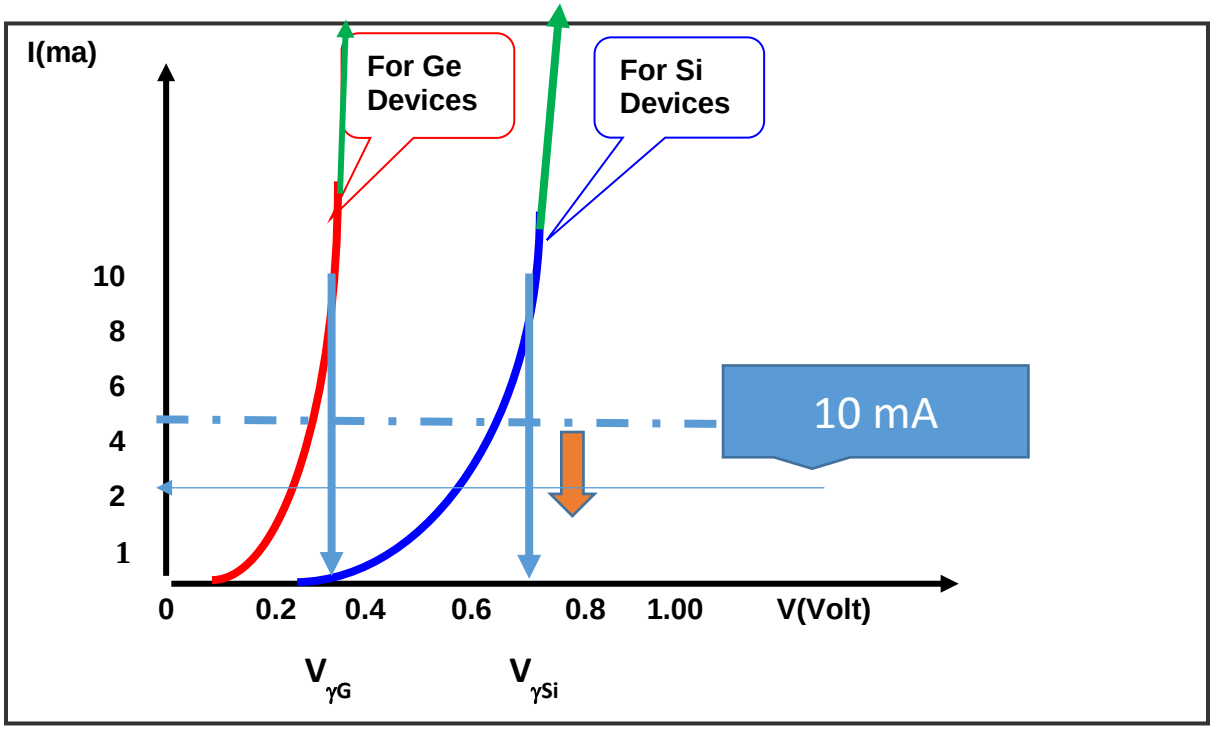
Solution



We deduce that, $\partial I/\partial t$ = 0.08% /^oC for Si, 0.11%/^oC for Ge, also we have found that the reverse saturation current increases by 7%/^oC for Ge, Si. We conclude that the reverse saturation current double it self-every 10^oC rise in temperature. The much larger value of the reverse saturation current for Ge than for Si, and since the temperature dependence is the same for both materials, then the elevated temperature in Ge devices will develop an excessive large reverse saturation current, where for Si, reverse saturation current will be quite modest. For more clarification, an increase in temperature from room temperature to 90 ^oC increases the reverse saturation current for Ge to hundreds of microamperes, in Si it rises to tenth of microamperes

Question (35)

How you can explain that at same applied voltage, the current in Ge diode is more than the current in Si diode?



As shown in figure, that at the same applied voltage, the current in Ge diode is greater than in Si diode, that is because the mobility of charge carriers in Ge diode is greater than in Si diode. Normally, $\mu_n > \mu_p$ for any material. For example, in silicon $\mu_n = 1800$, $\mu_p = 400$ cm^2/V. sec, and in germanium we find that $\mu_n = 3800$, $\mu_p = 1800$ cm^2/V. sec. The currents depended on the value of mobility. at same, applied voltage, the current in Ge diode is more than the current in Si diode

Question (36)

How we can express such expressions, Applied voltage (V_o) , built – in or , barrier voltage (V_T) , forward voltage (V_F) , reverse voltage (V_R) , cut-in or offset or break point or threshold voltage (V_γ) , Zener or breakdown voltage (V_Z)?

Solution

- **Applied voltage (V_o), is the battery voltage applied to in semiconductor diode circuit, it can be positive or negative to be forward or reverse.**
- **built – in or, barrier voltage (V_T), is the voltage that be built – up during the pn contact construction to hinder more diffusion of both charge carriers and bring the system in neutral electric mode.**
- **forward voltage (V_F), is the applied voltage to pn device, it decreases the barrier voltage and increase charge carrier concentration and bring the diode in forward bias mode.**
- **reverse voltage (V_R), is the applied voltage to pn device, it increases the barrier voltage and decrease charge carrier concentration and bring the diode in reverse bias mode.**
- **cut-in or offset or break point or threshold voltage (V_γ), is greater than the barrier voltage, it is in forward bias mode but below which forward below which forward current is very small, less than 1% of its maximum.**
- **Zener or breakdown voltage (V_Z) , is in reverse bias mode , when reverse voltage increases for a certain value , rush of reverse saturation current can damage the diode.**

Question (37)

How we can express such expressions, forward current (I_F), reverse current (I_R), reverse saturation current (I_S) cut-in current (I_γ) , Zener or breakdown current (I_Z)?

Solution

- **Forward current (I_F), in forward bias mode current flow between the diode terminal, it is due to majority charge carriers, this current depend on the forward voltage, it has nonlinear behavior at certain forward voltage, less more forward voltage then it has linear characteristic**
- **Reverse current (I_R), in reverse bias mode, the current between the diode terminal disappeared, it is due to minority charge carriers, this current is constant not depend on the reverse voltage.**
- **Reverse saturation current (I_S), in reverse bias mode, the current between the diode terminal disappeared, it is due to minority charge carriers, this current is constant not depend on the reverse voltage.**
- **Cut-in current (I_γ), in forward bias mode current flow between the diode terminal), it is due to few of majority charge carriers which has higher energy**

levels which ionized first before the ionization of large concentration of carriers, this current exist in the range of built -in voltage and cut-in voltage, its value is not more than 1% of the maximum forward current.

- Zener or breakdown current (I_Z), in reverse bias mode, the reverse saturation current is existing, it is due to minority charge carriers, this current is constant not depend on the reverse voltage until certain reverse voltage (V_Z). then higher current is flow; this current can damage the diode.

Question (38)

Which types of resistance, we have in the pn diodes?

Solution

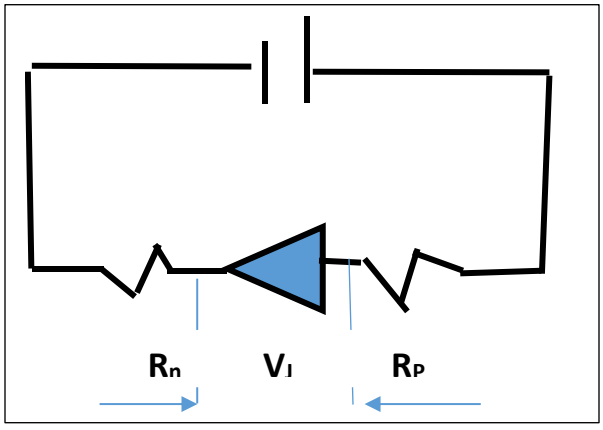
we have two possible resistances to consider:

- **DC resistance; Dc resistance of the modelling diode combination is**

$$R_{dc} = R_T - (R_n + R_p);$$

The Dc resistance of ideal part of diode, (r_{dc}) can be calculated from:

$$r_{dc} = \frac{V_J}{I_J} = \frac{V_J}{I_S \, exp\left[\frac{qV_J}{KT} - 1\right]}$$



- **Dynamic or small signal resistance (ac resistance) (r_a) an important parameter and it is equal,**

$$r_a = \frac{\partial V}{\partial I}$$

Dynamic resistance r_a is not constant depends upon the voltage and we find that the dynamic conductance for PN ideal diode is given by:

$$g = \frac{1}{R} = \frac{\partial I}{\partial V} = \frac{I_o e^{V/\eta V_T}}{\eta V_T} = \frac{I + I_o}{\eta V_T}$$

For reverse bias, where $V/\eta V_T << 1$, conductance g = 1/R will be very small and dynamic resistance r is very large. For forward bias, where $V/\eta V_T >> 1$, $I >> I_o$ and dynamic resistance r is given by:

$$r_a = \frac{\eta V_T}{I}$$

Ac resistance r_{ac} of ideal diode determined from slope of C.C at the operating points or determined analytically as follows. It is convenient to calculate ac conductance (g_{ac}),

$$I_J = I_S exp\left[\frac{qV_J}{KT} - 1\right]$$

Ac resistance of real diode is then,

$$R_{ac} = r_{ac} + R_n + R_p$$

$$R_{ac} = \frac{KT}{q}\left(\frac{1}{I_s + I_J}\right) + R_n + R_p$$

At room temperature, value of R_{ac},

$$r_{ac} = \frac{25}{I_s + I_J} ohm$$

Note that in some cases the ohmic series resistance will be important and in other is not. At very high current the forward ideal diode resistance becomes negligible compared with the series resistance. Since the series resistance in the real diode C.C becomes ohmic at high currents.

Question (39)

What are the parameters on which the junction current depend upon?

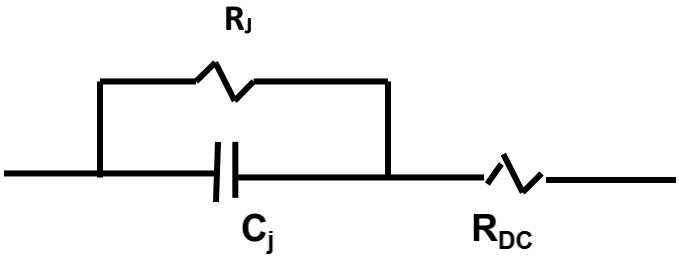
Solution

Parameters on which the junction current depend upon are: physical properties of the junction, properties of the crystal, density of impurities, impurity distribution, and many other factors.

Question (40)

Draw a complete equivalent circuit for P-N diode?

Solution



Total of the resistance combination is = R_{DC} in series with combination of junction resistance and capacitance which are in parallel connection

$$R_T = R_{DC} + (R_J \;//\; C_J) = (R_n + R_p) + (R_J \;//\; C_J)$$

C_J is the junction capacitance due to depletion layer which exhibits the behavior of a capacitance having the same geometry and dielectric constant.

$$qN_A\, x_p = qN_D x_n$$

Problem (1)

Write the electronic configuration of silicon has 14 electrons in its atom, determine in which sub shell and in which orbit and how many electrons in the highest sub shell energy.

Solution:

The electronic configuration of silicon as follows,

$$1S^2\ 2S^2\ 2p^6\ 3S^2\ 3p^2$$

The highest sub shell energy lies in (M) orbit, in the sub shell (p) which is not fully occupied, it has only 2 electrons

problem (2)

Calculate the conductivity and the resistivity of n-type silicon wafer, which contains 10^{16} electrons per cubic centimeter with an electron mobility of 1400 cm^2/Vs.

Solution:

The conductivity is obtaining by adding the product of the electronic charge, q, the carrier mobility, and the density of carriers of each carrier type, or:

$$\sigma = q\left(n\,\mu_n + p\,\mu_p\right)$$

As n-type material contains almost no holes, the conductivity equals:

$$\sigma = q\,n\,\mu_n = 1.6\,x\,10^{-19}\,x\,1400\,x\,10^{16} = 2.24\;\; 1\Omega cm$$

The resistivity equals the inverse of the conductivity

$$\rho = \frac{1}{\sigma} = \frac{1}{q\left(n\,\mu_n + p\,\mu_p\right)}$$

In addition, equals ρ = 1/ σ = 1/2.24 = 0.446 Ω cm

Problem (3)

A silicon wafer contains 10^{16} cm^{-3} electrons. Calculate the hole density and the position of the intrinsic energy and the Fermi energy at 300 K. Draw the corresponding band diagram to scale, indicating the conduction and valence band edge, the intrinsic energy level and the Fermi energy level. Use $n_i = 10^{10}$ cm^{-3}.

Solution:

The hole density is obtained using the mass action law:

$$p = \frac{n_i^2}{n} = \frac{10^{20}}{10^{16}} = 10^4\,cm^{-3}$$

The position of the intrinsic energy relative to the mid gap energy equals:

$$E_i - \frac{E_c + E_v}{2} = -\frac{3}{4} KT\, ln\, \frac{m_h^*}{m_e^*} = \frac{3}{4}\, x\, 0.0258\, ln\, \frac{0.81}{1.08} = 5.58\, meV$$

The position of the Fermi energy relative to the intrinsic energy equals:

$$E_F - E_i = KT\, ln\left(\frac{N_d}{n_i}\right) = 0.0258\, ln\, \frac{10^{16}}{10^{10}} = 357\, meV$$

Problem (4)

A piece of silicon has a resistivity which is specified by the manufacturer to be between 2 and 5 Ohm cm. If the mobility of electrons is 1400 cm^2/V-sec and that of holes is 450 cm^2/V-sec, what is the minimum possible carrier density and what is the corresponding carrier type? Repeat for the maximum possible carrier density.

Solution

The minimum carrier density obtained for the highest resistivity and the material with the highest carrier mobility, i.e. the n-type silicon. The minimum carrier density therefore equals:

$$n = \frac{1}{q\, \mu_n \rho_{max}} = \frac{1}{1.6\, x\, 10^{-19}\, x\, 1400 x\, 5} = 8.92\, x\, 10^{14} cm^{-3}$$

The maximum carrier density obtained for the lowest resistivity and the material with the lowest carrier mobility, i.e. the p-type silicon. The maximum carrier density therefore equals:

$$p = \frac{1}{q\, \mu_p\, \rho_{max}} = \frac{1}{1.6\, x\, 10^{-19}\, x\, 450 x\, 2} = 6.94\, x\, 10^{15} cm^{-3}$$

Problem (5)

Calculate the intrinsic carrier density in silicon at 300, 400, 500 and 600 °K. if the effective density of electrons in conduction band is $2.81\, x\, 10^{19}$ and the effective density of holes in valance band is $1.83\, x\, 10^{19}$.

Solution

The intrinsic carrier density in silicon at 300 °K equals:

$$n_i(300K) = \sqrt{N_c N_v}\, exp\left(\frac{-E_g}{2\,KT}\right)$$
$$= \sqrt{2.81\ x\ 10^{19}\ x\ 1.83\ x\ 10^{19}}\, exp\ \left(\frac{-1.12}{2\ x\ 0.0258}\right)$$
$$= 8.72\ x\ 10^{9} m^{-3}$$

To get the value of T differ than room temperature (300 °K) , and since Boltzmann constant is not given , so we can get the required value from the ratio between the value of KT at 300 °K (0.026 eV) and its value at 400 °K ,

- **At 300 °K = 0.026 eV , then KT at 400 °K is 400 x 0.026 / 300 = 0.0346 eV**

So,

$$n_i(400K) = \sqrt{N_c N_v}\, exp\left(\frac{-E_g}{2\,KT}\right)$$
$$= \sqrt{2.81\ x\ 10^{19}\ x\ 1.83\ x\ 10^{19}}\, exp\ \left(\frac{-1.12}{2\ x\ 0.0346}\right)$$
$$= 4.52\ \text{x}\ 10^{12}\ \ electrons\ in\ m^{-3}$$

- **At 300 °K = 0.026 eV , then KT at 500 °K is 500 x 0.026 / 300 = 0.0433 eV**
  - $n_i(500K) = \sqrt{N_c N_v}\, exp\left(\frac{-E_g}{2\,KT}\right) = \sqrt{2.81\ x\ 10^{19}\ x\ 1.83\ x\ 10^{19}}$

$$exp\ \left(\frac{-1.12}{2\ x\ \ 0.0433}\right) = 2.16\ \text{x}\ 10^{14}\ \ electrons\ in\ m^{-3}$$

- **At 300 °K = 0.026 eV , then KT at 600 °K is 400 x 0.026 / 300 = 0.052 eV**

$$n_i(600K) = \sqrt{N_c N_v}\, exp\left(\frac{-E_g}{2\,KT}\right) = \sqrt{2.81\ x\ 10^{19}\ x\ 1.83\ x\ 10^{19}}$$

$$exp\ \left(\frac{-1.12}{2\ x\ \ 0.052}\right) = 3.07\ \text{x}\ 10^{15}\ \ electrons\ in\ m^{-3}$$

Temperature °K	300	400	500	600
Intrinsic concentration	$8.72 \text{ x } 10^{9}$	$4.52 \text{ x } 10^{12}$	$2.16 \text{ x } 10^{14}$	$3.07 \text{ x } 10^{15}$
Change % above RT	-----	5.183 %	247.7%	3520%